Master's Thesis

STUDY OF FULLY-INTEGRATED LOW-DROPOUT REGULATORS

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Approved by

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Abstract

This thesis focuses on the introduction of fully-integrated low-dropout regulators (LDOs). Recently, for the mobile and internet-of-things applications, the level of integration is getting higher. LDOs gets popular in integrated circuit design including functions such as reducing switching ripples from high-efficiency regulators, cancelling spurs from other loads, and giving different supply voltages to loads. In accordance with load applications, choosing proper LDOs is important. LDOs can be classified by the types of power MOSEFT, the topologies of error amplifier, and the locations of dominant pole. Analog loads such as voltage-controlled oscillators and analog-to-digital converters need LDOs that have high power-supply-rejection-ratio (PSRR), high accuracy, and low noise. Digital loads such as DRAM and CPU needs fast transient response, a wide range of load current providable LDOs. As an example, we present the design procedure of a fully-integrated LDO that obtains the desired PSRR. In analog LDOs, we discuss advanced techniques such as local positive feedback loop and zero path that can improve stability and PSRR performance. In digital LDOs, the techniques to improve transient response are introduced. In analog-digital hybrid LDOs, to achieve both fast transient and high PSRR performance in a fully-integrated chip, how to optimally combine analog and digital LDOs is considered based on the characteristics of each LDO type. The future work is extracted from the considerations and limitations of conventional techniques.

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Technical Terms and Abbreviations

IoT	Internet of things
SoC	System on a chip
PMIC	Power management integrated circuit
LDO	Low-dropout voltage regulator
PSRR	Power supply rejection ratio
GPD	Gate pole dominant
OPD	Output pole dominant
UGF	Unity gain frequency
ESR	Equivalent series resistance
BGR	Band gap reference
DVFS	Dynamic voltage and frequency scaling
LSB	Least significant bit
PZC	Pole-zero cancellation
FVF	Flipped-voltage-follower

I. INTRODUCTION

For the mobile and internet-of-things (IoT) applications, the compact integration and low power dissipation is necessary in chip design. System-on-chip (SoC) that is contained every function in a compact chip become popular since it can remove chip-to-chip path-caused parasitic by removing power and signal delivery between chips. According this tendency, power management integrated circuits (PMICs) should be fully-integrated and thus more complex strategies are needed when designing these circuits.

As shown in the top of Figure 1, a battery provides charges to the inputs of DC/DC converters and these converters deliver supply voltages to loads containing charges in capacitors ($C_{L,DC/DC}$s) as the level of desired voltage. However, these supplies contain large switching ripples by the operation properties of these converters and spurs from other loads sharing same supply voltage. These problems make the loads which need clean and noise-less supply cannot operate properly. Furthermore, the loads can operate optimally in their own supply voltage level but DC/DC converters only provide same voltage level to their loads.

To resolve these problems, low-dropout voltage regulators (LDOs) are added between switching converters and loads as shown in the bottom of Figure 1. Even if the LDOs have lower power efficiency than DC/DC converters due to series connection on current provision path, they can suppress switching ripples from DC/DC converters, reduce spurs from other loads, and provide different supply voltage to the different loads.

As shown in Table 1, different types of voltage regulators can be used considering the condition of load blocks [1]. Since LDOs can rapidly provide the desired current to the load with less noise, it can be preferred loads which want that kinds of properties. The objective of LDOs is that they are seen as an ideal voltage source. It means that the LDO should provide exact output voltage (V_{OUT}) level to their loads and the level should not be fluctuated by itself or sudden load transition. In other words, it should response rapidly to the change of load current (I_L) and supply of LDO (V_{IN}). LDOs were usually introduced to reduce the noise of DC/DC converters and keep loads from supply coupling in analog loads such as voltage-controlled oscillators (VCOs) and analog-to-digital converters (ADCs), but in recent years, they are used to provide wide range of I_L and rapidly compensating frequent I_L steps to keep the supply of digital loads such as DRAM and CPU.

In this thesis, we present the fundamentals of LDOs such as operation and performance metrics of LDOs in Chapter II. In Chapter III, design and simulations of a fully-integrated analog LDO is

introduced. We bring out the future work of LDO in Chapter IV and make conclusion in Chapter V.

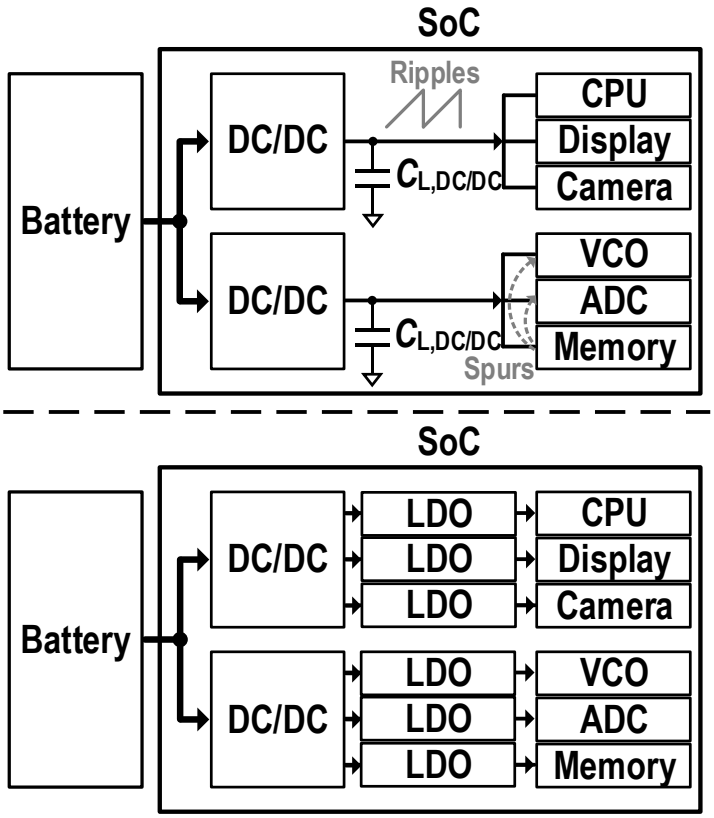


Figure 1. The path of charge delivery from a battery to loads without LDOs (top) and with LDOs (bottom).

Table 1. Comparison of voltage regulators

	Linear regulator	**Switching regulator**
Efficiency	Low	High
Noise	Low	High
Transient response	Fast	Slow
Step-up voltage	No	Yes
Step-down voltage	Yes	Yes
Area	Small	Large

II. FUNDAMENTALS OF LOW-DROPOUT REGULATORS (LDOS)

2.1 BASIC OF LDOS

2.1.1 Operation of LDOs

As shown in Figure 2, analog LDOs basically consist of a P-type pass transistor (M_P), an error amplifier (EA), and a load capacitor (C_L). If I_L or V_{IN} changes, C_L compensates the change firstly occurring fluctuation in V_{OUT}. In the second step, feedback loop operates to regulate M_P current (I_{OUT}) as the same value of I_L, restoring V_{OUT} same value with reference voltage (V_{REF}).

For example, as shown in the top of Figure 3, when I_L changes from minimum I_L ($I_{L,min}$) to maximum I_L ($I_{L,max}$), the current from C_L (I_{CL}) initially compensates I_L, and it evokes V_{OUT} decrease. After that, the negative feedback loop operates: input difference of EA decreases by V_{OUT} decreasing and the reduction is amplified with EA gain (A_{EA}), evoking huge decrease of the gate node voltage (V_G) of M_P. This increase of $|V_{GS}|$ of M_P results in huge increase of I_{OUT}, so M_P can provide current in the same quantity with I_L, and thus put V_{OUT} on almost same value with V_{REF}. As shown in the bottom of Figure 3, when I_{CL} compensates I_L initially, V_{OUT} decreases, but as the portion of I_{OUT}–compensation increases, V_{OUT} gets back to the value of V_{REF}.

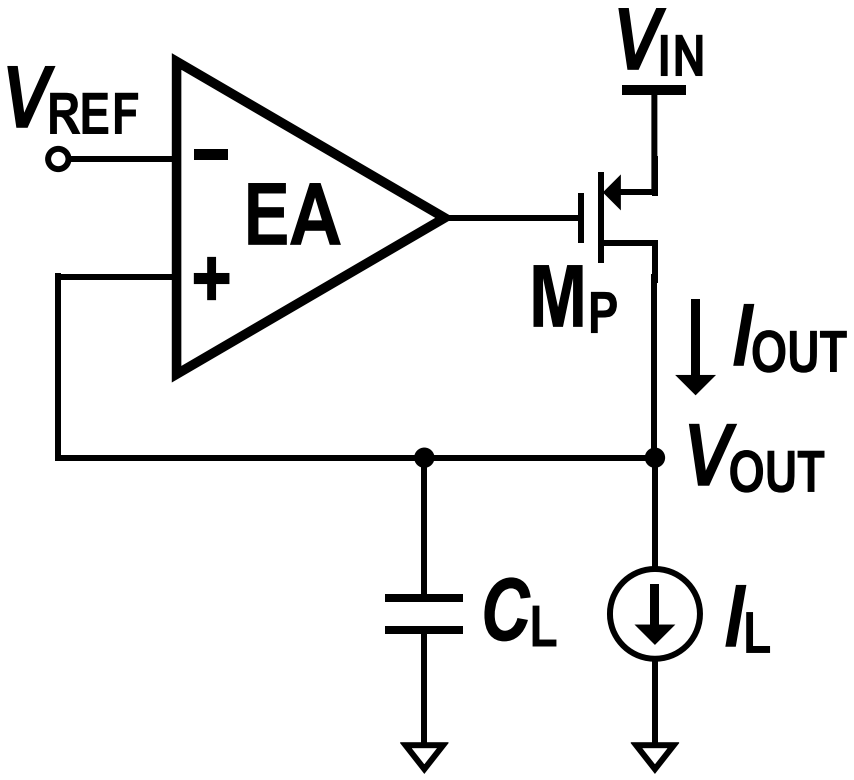
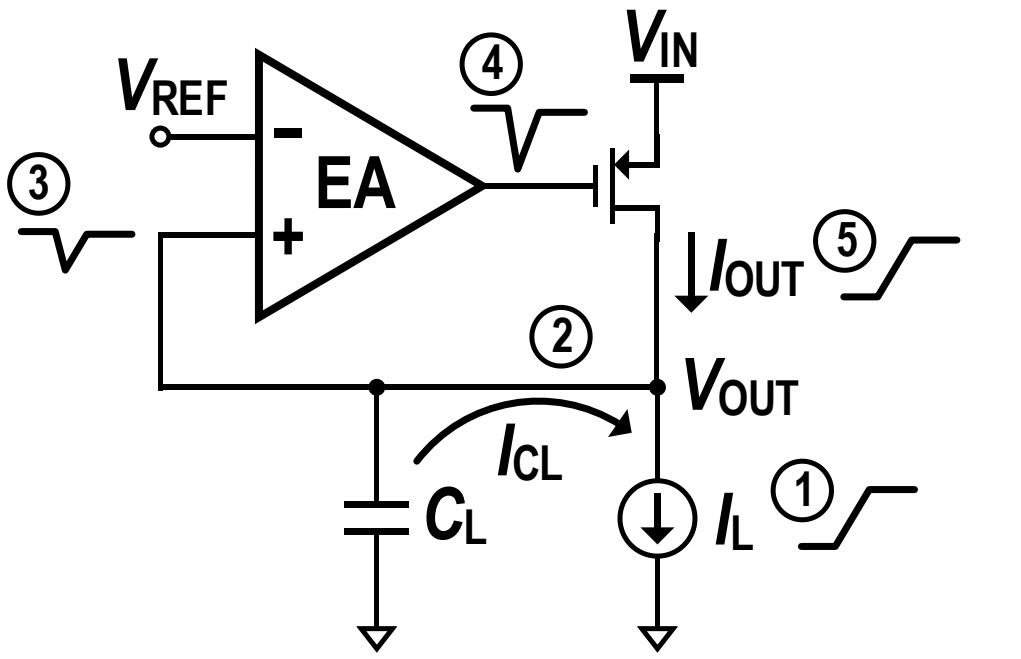


Figure 2. Basic structure of analog LDO



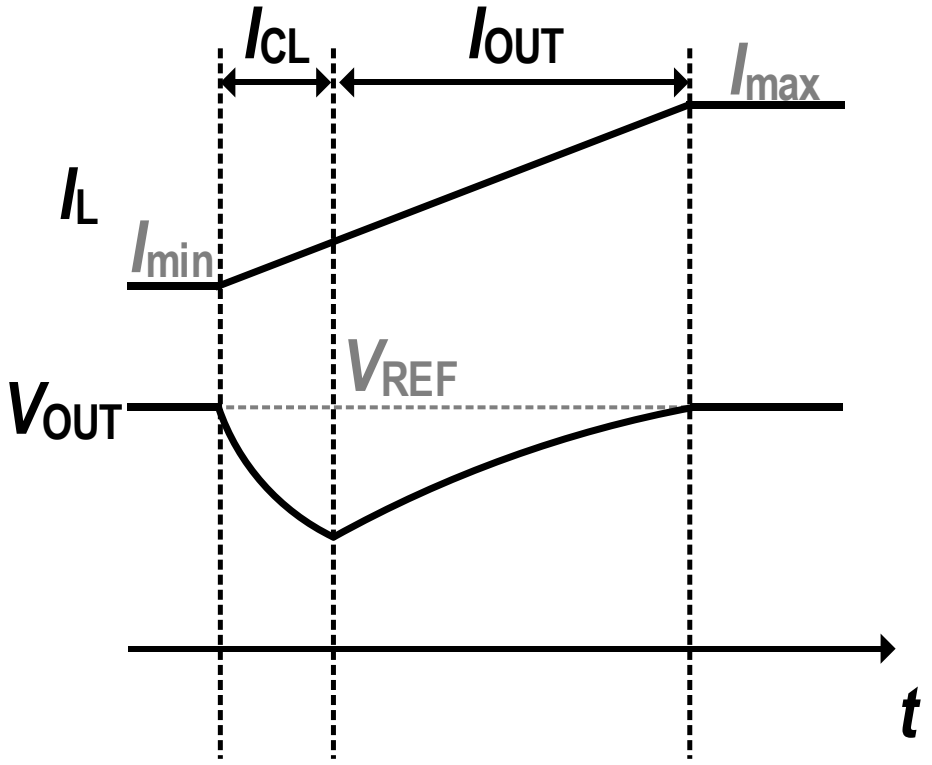


Figure 3. LDO operation when I_L changes from $I_{L,min}$ to $I_{L,max}$.

2.1.2 Types of Pass Transistor

We need to select the type of pass transistor between P-type and N-type for desired purpose. M_P has smaller dropout voltage (V_{DO}), lower power supply rejection ratio (PSRR), and lower output pole frequency ($\omega_{P,OUT}$) than N-type pass transistor (M_N). The comparison of pass transistor type is shown in Table 2.

V_{DO} is the dropout voltage between V_{IN} and V_{OUT}. As shown in Figure 4, For M_N operating in saturation region, V_{DO} should be large. Otherwise, V_G should be larger than V_{IN}. Because V_G should be larger than the sum of V_{OUT} and threshold voltage (V_{th}) of M_N. For example, if V_{th} of M_N is over 300mV and the specification needs under 200mV V_{DO}, charge pump is needed for increasing V_G as larger than V_{IN} + 100mV.

PSRR is the ratio of the change in V_{IN} to the change in V_{OUT} it produces. If V_{IN} fluctuates, in M_N case, V_{OUT} is robust to V_{IN} fluctuation since in view of V_{OUT}, only drain of M_N fluctuates and MOSFET is inherently robust to the change of V_{DS}. However, M_P amplifying as M_P gain (A_{MP}) and deliver to V_{OUT} since the change occurs in V_{GS}. Thus, we generally say M_N type LDOs have high PSRR than M_P type LDOs. However, it is just a part of tendency and if deep analysis is conducted, the solution will be ambiguous. Detail strategies are presented in Section 2.2.1. In brief, after determining the type of pass transistor, EA type should be selected as the way v_R cannot be represented in V_{OUT} [2].

General structure of LDO has two low frequency poles. $\omega_{P,OUT}$ is the pole at the node of V_{OUT}, and $\omega_{P,G}$ is the pole at the node of V_G. In M_N case, since low $1/g_m$ impedance of M_N is seen by V_{OUT}, $\omega_{P,OUT}$ can easily be higher than $\omega_{P,G}$ and makes LDO gate-pole-dominant (GPD). However, in M_P case, since the high r_O impedance of M_P is seen by V_{OUT}, it can be negligible, so by the condition of load impedance, it can be GPD or output-pole-dominant (OPD) LDO. The characteristics of GPD and OPD LDO are explained in Section 2.1.3.

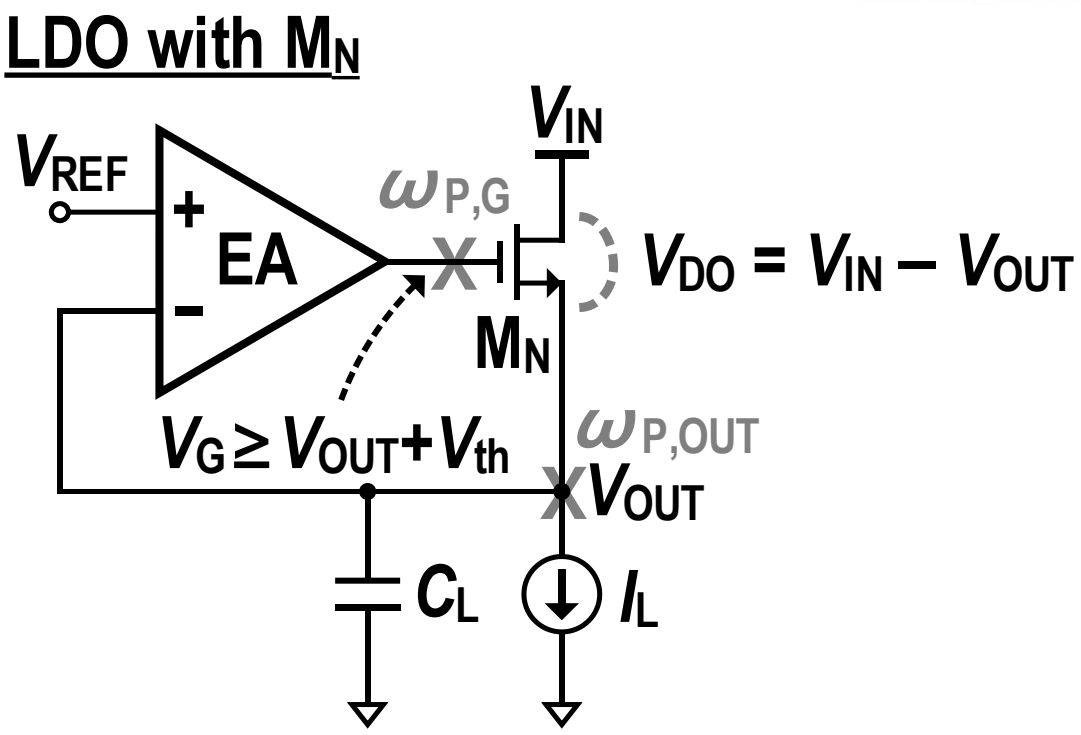


Figure 4. Analog LDO with M_N

Table 2. Comparison between M_P and M_N

Pass transistor type	**P-type (M_P)**	**N-type (M_N)**
V_{DO}	Low	High
PSRR	Low	High
$\omega_{P,OUT}$	Depend on I_L	High

2.1.3 Location of Dominant Pole

Location of dominant pole is important consideration. In the past years, almost all LDOs were OPD since designers use large off-chip capacitor so $\omega_{P,OUT}$ is near to DC making feedback loop stable even in the situation that $\omega_{P,G}$ is somewhat small. Moreover, this large C_L can bypass the noise of LDOs, and can be robust to load transition since the large C_L compensates most I_L with little fluctuation of V_{OUT} (ΔV_{OUT}).

However, in recent years, fully-integrated LDOs are required to reduce PCB area and the number of pins in chips. As C_L size is reduced, satisfying stability condition becomes difficult in OPD LDOs. In some applications, over 10mA I_L is needed. For these reasons, GPD LDOs get popular for fully-integrated design. The differences between OPD and GPD LDOs are summarized in Table 3.

Table 3. Comparison of GPD and OPD LDOs

Location of dominant pole	**Gate**	**Output**
Area	Small	Large
Noise	High	Low
ΔV_{OUT}	High	Low
Stability @ $I_{L,min}$	Poor	Good
Stability @ $I_{L,max}$	Good	Poor

2.2 PERFORMANCE METRICS OF LDOS

2.2.1 Power-Supply Rejection Ratio (PSRR)

DC/DC converter ripple compression is one of the most significant goals of LDOs. Figure 5 shows two paths that v_R are delivered to V_{OUT} [3]. First path is through drain–source resistance of M_P ($1/g_{ds}$) directly. Second path is through V_G. In the second path, V_G takes portion of the v_R by impedance dividing. The difference between V_G and V_S is amplified to V_{OUT} by the transconductance of M_P (g_m), so removing the difference is necessary. We can represent two paths with the equation that is related with change of I_{OUT} (ΔI_{OUT}) as

$$\Delta I_{OUT} = g_{ds} \cdot v_R + g_m \cdot \left(v_R - v_R \cdot \frac{C_{gs}}{C_{gs} + C_{gd}} \right) \quad (1)$$

where g_{ds} is the drain-source conductance of M_P, C_{gs} is the gate-source capacitance of M_P, and C_{gd} is the gate-drain capacitance of M_P.

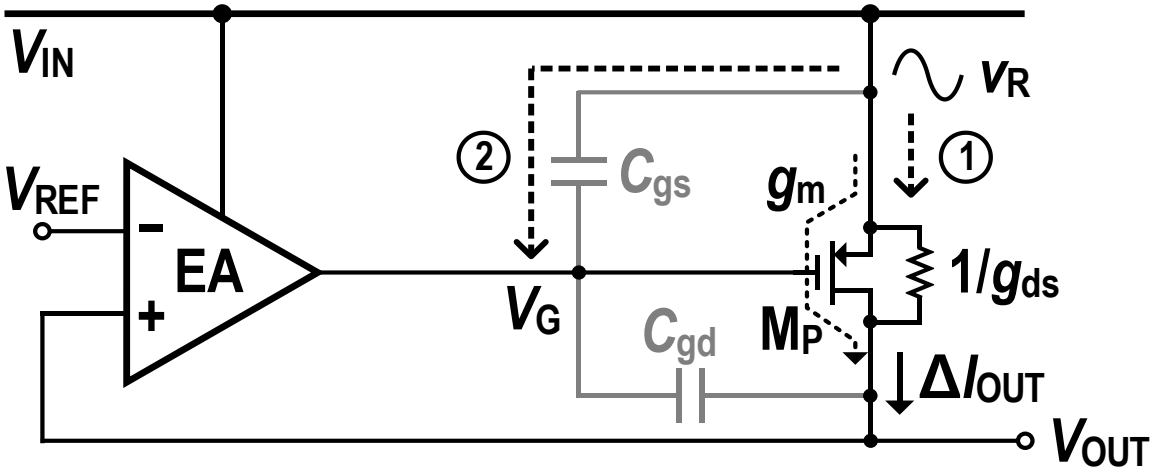


Figure 5. The paths that v_R are represented to V_{OUT}.

As mentioned in Section 2.1.2, in the path related to the first term of (1), v_R are multiplied by g_m in the M_P case, and multiplied by $1/r_o$ in the M_N case. However, in the second path, the ratio between C_{gs} and C_{gd} dominantly determines the fluctuation of ΔI_{OUT}. In the M_P case, increasing C_{gs} (between V_G and V_{IN}) helps improve PSRR performance and in the M_N case, increasing C_{gs} (between V_G and V_{OUT}) helps improve PSRR performance. Plus, we should consider the situation that v_R affect the output of EA and generates V_G ripples. The solution for this problem is provided in [2].

As shown in Figure 6–7, (2), and (3), we can remove these ripples by selecting suitable structure of EA. Briefly, for maximizing v_R to V_G fluctuating, PMOS mirror can be selected as it delivers the current that affects V_G in the same direction of resistive dividing path. In the opposite case, NMOS mirror can

affect V_G in the opposite direction of resistive dividing path. It is worth noting that before-mentioned techniques are only applied to improve PSRR in the low frequency band.

Figure 8 shows PSRR along frequency in the LDO that includes M_P and NMOS input PMOS mirror EA combination. In DC region, PSRR has the value $A_{EA} \cdot A_{MP}$ (A_{OL}). If the frequency over –3dB bandwidth (BW_{-3dB}) of loop that is $\omega_{P,G}$, A_{EA} is reduced and PSRR performance gets degradation. In OPD LDO case, the PSR is kept constant since the load impedance rolls-off not only A_{EA} does. To return to the GPD LDO case, if the frequency over the unity gain frequency (UGF), there is no more gain from EA, so the PSRR is kept constant. If the frequency over the output pole, load impedance rolls off, so the PSRR increases. If the frequency over the BW_{-3dB} of load impedance that is made by C_L and equivalent series resistance (R_{ESR}) of the C_L, load impedance remains constant, so the PSRR is kept constant.

The BW_{-3dB} of PSRR (p_1) can be more important than $PSRR_{DC}$ in the situation high frequency spur is injected into V_{IN} such as the optical receiver applications [4]. Then, we can flip the combination from $PSRR_{DC}$ desiring combination. The characteristics of combinations are summarized in Table 4.

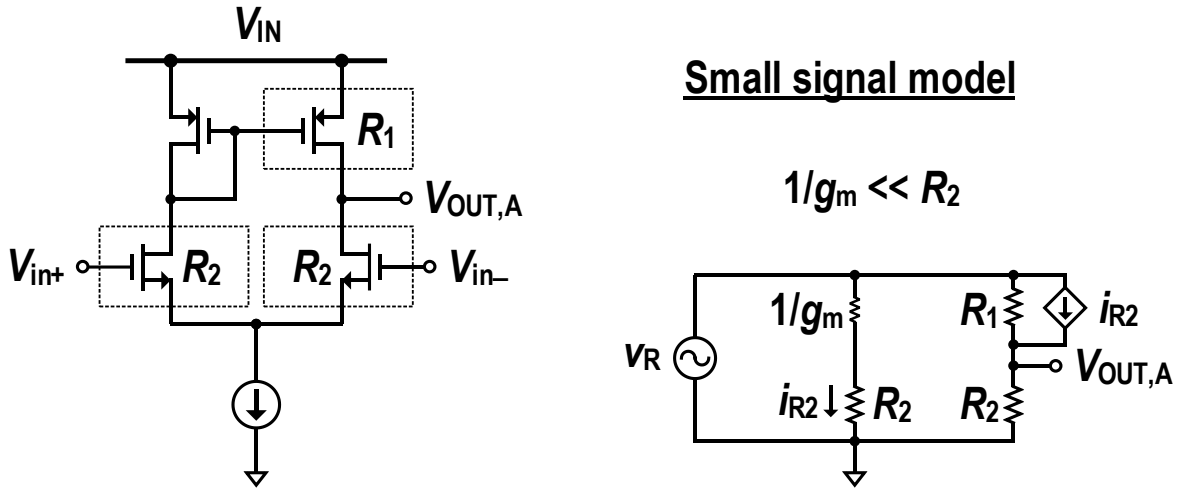


Figure 6. Delivering v_R to EA output fully in NMOS-input, PMOS-mirror.

$$V_{OUT,A} = v_R \cdot \frac{R_2}{R_1 + R_2} + i_{R2}(R_1 || R_2)$$
$$\approx v_R \cdot \frac{R_2}{R_1 + R_2} + \frac{v_R}{R_2}\left(\frac{R_1 R_2}{R_1 + R_2}\right) = v_R \quad (2)$$

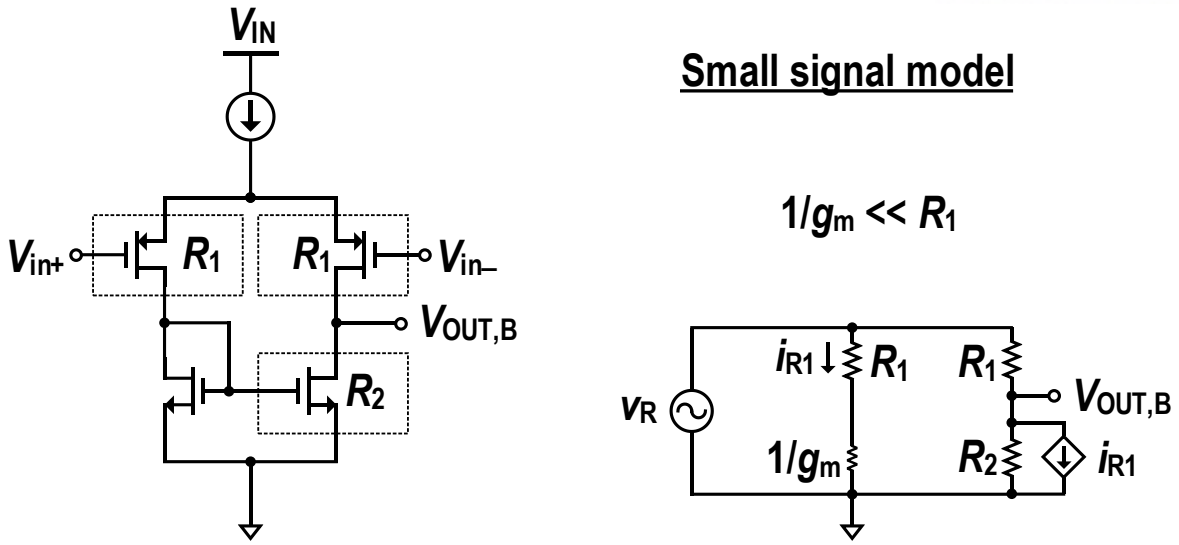


Figure 7. Delivering v_R to EA output scarcely in PMOS-input, NMOS-mirror.

$$V_{OUT,B} = v_R \cdot \frac{R_2}{R_1 + R_2} - i_{R1}(R_1||R_2)$$
$$\approx v_R \cdot \frac{R_2}{R_1 + R_2} - \frac{v_R}{R_1}\left(\frac{R_1 R_2}{R_1 + R_2}\right) = 0 \quad (3)$$

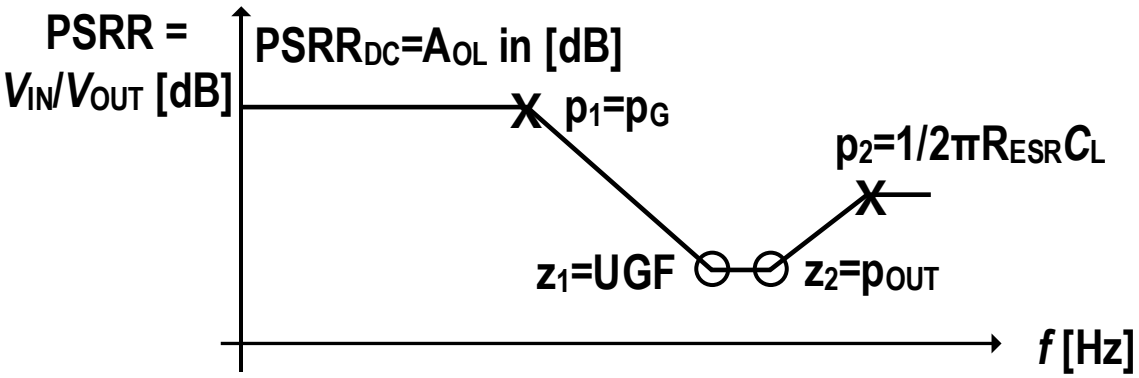


Figure 8. PSR change along frequency.

Table 4. The characteristics of combinations

Pass transistor type	**EA**	**$PSRR_{DC}$**	**p_1**
M_P	NMOS input PMOS mirror	A_{OL}	p_G
	PMOS input NMOS mirror	A_{EA}	$A_{MP}p_G$
M_N	NMOS input PMOS mirror	A_{EA}	$A_{MP}p_G$
	PMOS input NMOS mirror	A_{OL}	p_G

2.2.2 Output Voltage Noise ($V_{n,rms}$)

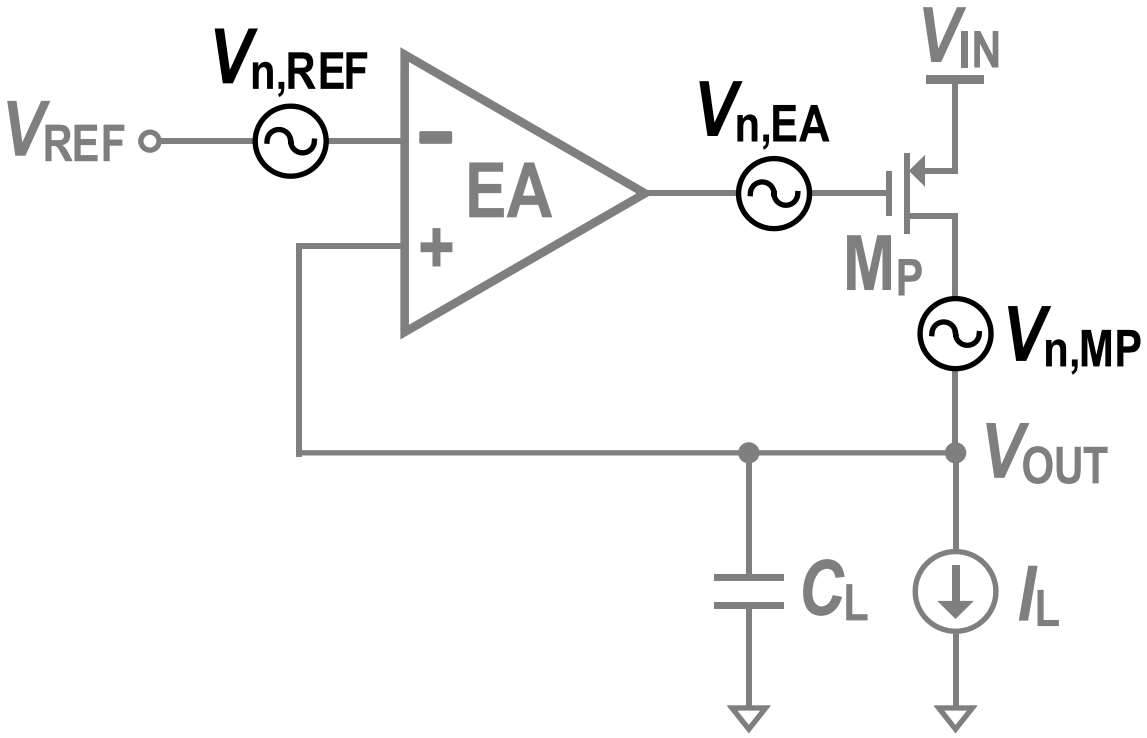


Figure 9. Different noise sources of LDOs

Output voltage noise ($V_{n,rms}$) is the total noise at the output node generated by a LDO itself. In some applications such as passive sensors, $V_{n,rms}$ becomes an important factor. Different noise sources are represented in Figure 9. V_{REF} noise ($V_{n,REF}$) comes from band-gap-reference (BGR) circuit, EA noise ($V_{n,EA}$) comes from EA, and M_P noise ($V_{n,MP}$) comes from M_P. $V_{n,REF}$ and $V_{n,EA}$ are dominant noise sources since they are amplified passing through the loop [5]. To suppress $V_{n,REF}$, a bypass capacitor at the node of V_{REF} can be added. An effective way to reduce $V_{n,rms}$ is to increase the value of C_L sacrificing the chip area. The types of noise sources are thermal noise and flicker noises. We can calculate the value with

$$\overline{V_{n,thermal}^2} = 4\mathrm{kTR}\cdot\frac{1}{1+\frac{s}{\omega_P}}$$
$$\overline{V_{n,flicker}^2} = \frac{K}{C_{ox}\mathrm{WL}}\cdot\frac{1}{f} \quad (4)$$

where k is Boltzmann's constant, T is the resistors' absolute temperature, R is resistance, K is the process-dependent constant, C_{ox} is the oxide capacitance in MOSFET devices, and W and L is channel width and length, respectively.

2.2.3 Line & Load Regulation

The line and load regulation are important specifications for LDO providing exact the level of V_{OUT}. Although the V_{IN} or I_L changes, V_{OUT} should be kept as the same value with V_{REF}. In the cover range of LDOs, the steady-state difference between V_{OUT} and V_{REF} by changing V_{IN} and I_L can be measured and related performance metrics are called line and load regulation, respectively. If a system needs dynamic voltage and frequency scaling (DVFS), line and load regulation of the LDO should be fine to provide desired levels. Some DVFS chips need <10mV resolution [6]. The line and load regulation performance of LDO using M_P can be increased by increasing A_{OL} as shown in (5) and (6).

$$\text{Line regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} = \frac{\left(\frac{r_{ds} \| R_L}{A_{EA} A_{MP}}\right)}{r_{ds} + \left(\frac{r_{ds} \| R_L}{A_{EA} A_{MP}}\right)} \approx \frac{\frac{R_L}{A_{OL}}}{r_{ds} + \frac{R_L}{A_{OL}}} \approx \frac{R_L}{r_{ds} A_{OL}} \tag{5}$$

$$\text{Load regulation} = \frac{\Delta V_{OUT}}{\Delta I_L} = \frac{r_{ds} \| R_L}{1 + A_{EA} A_{MP}} \approx \frac{R_L}{A_{OL}} \tag{6}$$

2.2.4 Load Transient Response Time (T_R) & Settling Time (T_S)

As mentioned in Section 2.1.1, if the I_L changes from light to heavy, C_L initially compensates the current, and V_{OUT} falls. After that, feedback loop operates with the speed of loop bandwidth and since I_{OUT} at that time can provide same quantity of current with I_L, the V_{OUT} can be same with V_{REF}.

T_R is defined as the time for the changed V_{OUT} to be compensated and head toward the direction of the desired value. In Figure 10, (7), and (8), the calculation of T_R is introduced according to the relationship between T_R and I_L transition time (T_{edge}) where t_0 is the moment at which the I_L changes [7]. T_S is defined as the time that V_{OUT} that deviates from V_{REF} returns back near V_{REF}, typically entering the range of 2% error with V_{REF}. In Figure 11, the metrics are marked on the graph of V_{OUT} transition.

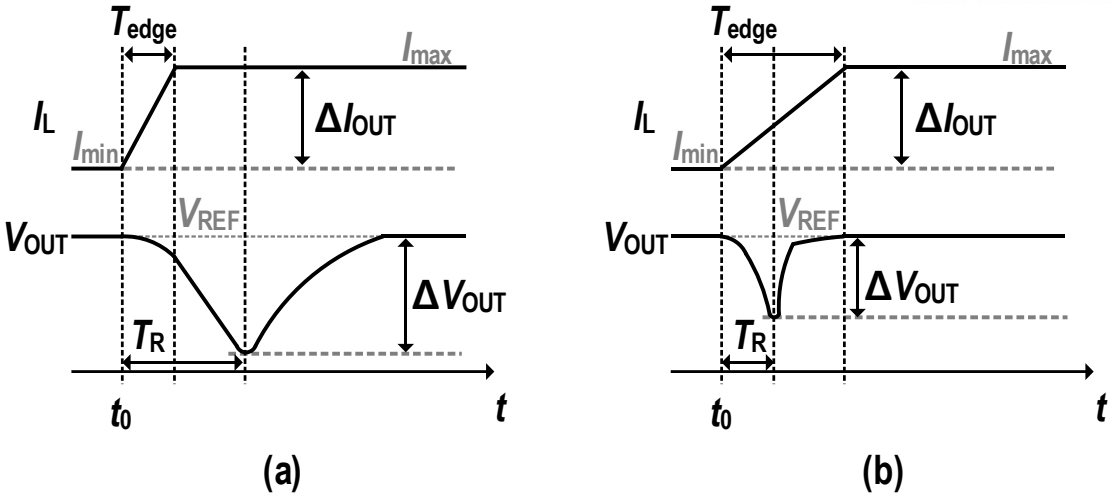


Figure 10. T_R when (a) $T_{edge} << T_R$ and (b) $T_{edge} > T_R$

$$\Delta V_{OUT} = \frac{1}{C_L}\left(\int_{t_0}^{t_0+T_{edge}} \Delta I_{OUT}(t)\,dt + \int_{t_0+T_{edge}}^{t_0+T_R} \Delta I_{OUT}\,dt\right) \approx \frac{\Delta I_{OUT} T_R}{C_L} \tag{7}$$

$$\Delta V_{OUT} = \frac{1}{C_L}\int_{t_0}^{t_0+T_R} \Delta I_{OUT}(t)\,dt,$$

$$\Delta V_{OUT} = \frac{T_R \Delta I_{OUT}(t)}{2C_L}\Big|_{t=T_R},$$

$$\Delta I_{OUT}(t)|_{t=T_{edge}} = \Delta I_{OUT} \rightarrow \frac{dI_{OUT}}{dt} = \frac{\Delta I_{OUT}}{T_{edge}} \rightarrow \Delta I_{OUT}(t)|_{t=T_R} = \frac{\Delta I_{OUT} T_R}{T_{edge}},$$

$$T_R = \sqrt{\frac{2C_L \Delta V_{OUT} T_{edge}}{\Delta I_{OUT}}} \tag{8}$$

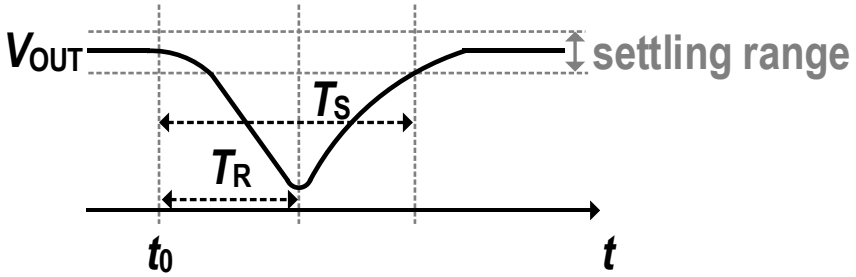


Figure 11. T_R and T_S when load transient.

2.2.5 Dropout Voltage (V_{DO}) & Quiescent Current (I_Q)

Quiescent current (I_Q) is defined as the difference between input and output currents of LDO [8]. I_Q is shown in Figure 12 and (9).

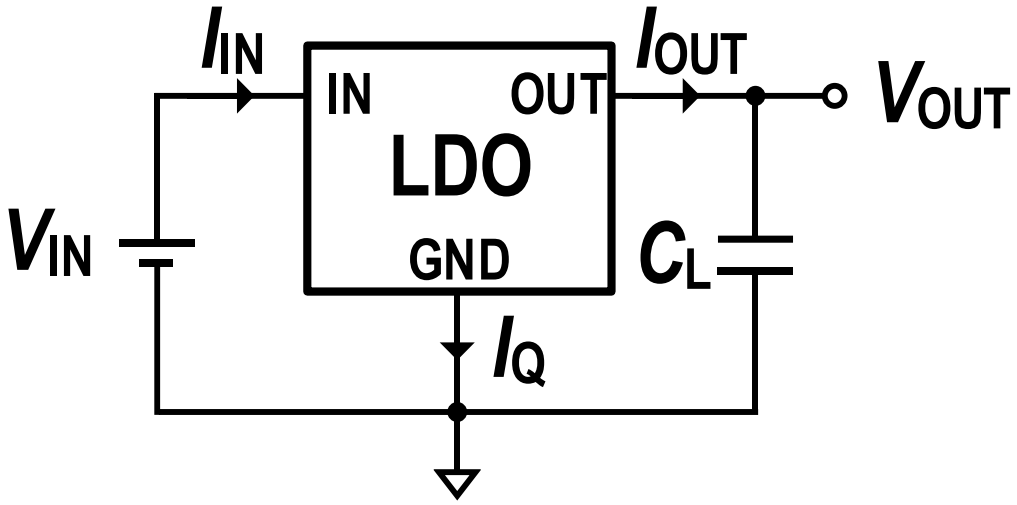


Figure 12. I_Q in LDO.

$$I_Q = I_{IN} - I_{OUT} \tag{9}$$

V_{DO} and I_Q are the metrics related to the power of LDO. These metrics are important for battery-based applications since power reduction can prolong the battery life. The power efficiency of LDO can be written as

$$\begin{aligned} \text{Power efficiency} &= \frac{I_{OUT}V_{OUT}}{(I_{OUT}+I_Q)V_{IN}} \times 100 \\ &= \eta_I \left(1 - \frac{V_{DO}}{V_{IN}}\right) \times 100 \end{aligned} \tag{10}$$

where η_I is the current efficiency. The focus whether reducing V_{DO} or reducing I_Q can be judged by the load condition. If the $I_{L,max}$ is huge and LDO usually operate in heavy load condition, reducing V_{DO} is more effective for reducing power. However, if the load operates usually in light load condition, the η_I will affect overall power significantly, so I_Q will be more important. It depends on how long the LDO stays in ON state and how much I_L is needed averagely. Designers can observe the load characteristics carefully and adopt right strategies.

2.2.6 Phase Margin (PM)

Stability is necessary condition for many circuits. The PM is the difference between the phase at UGF of a system and 180° implying how much the system is stable. Especially in LDOs, as the I_L varies from $I_{L,min}$ to $I_{L,max}$, the $\omega_{P,OUT}$ changes dynamically. Satisfying desired PM performance at the worst case brings lots of degradation of other performances such as lower accuracy, lower PSRR, lower transient responses. Thus, we need more advanced methods than designs that other performance metrics are limited by worst case of stability. The solution is making the parameters that affects stability adaptively change as the $\omega_{P,OUT}$ changes.

Light I_L makes GPD LDO unstable as shown in Figure 13. In [9], the LDO includes V_G sensing block. If V_G gets high, the block reduces the bias current of EA (I_B). Thus, at $I_{L,min}$, the LDO can keep stability without the reduction of the BW in heavy load condition. It is shown in Figure 14.

Heavy I_L makes OPD LDO unstable as shown in Figure 15. In [10], by dividing EA into EA' and a small gain amplifier, isolating the large output resistance of EA ($R_{OUT,EA}$) from the large total capacitance of M_P seen from gate (C_{gg}). Plus, for reduced gain because of EA' ($A_{EA'}$), the small gain amplifier compensates the gain as $A_{EA}/A_{EA'}$ to make the total DC gain same with conventional EA. Thus, the LDO can keep stability just splitting the large resistance and capacitance without extra power consumption to push $\omega_{P,G}$ away. It is shown in Figure 16.

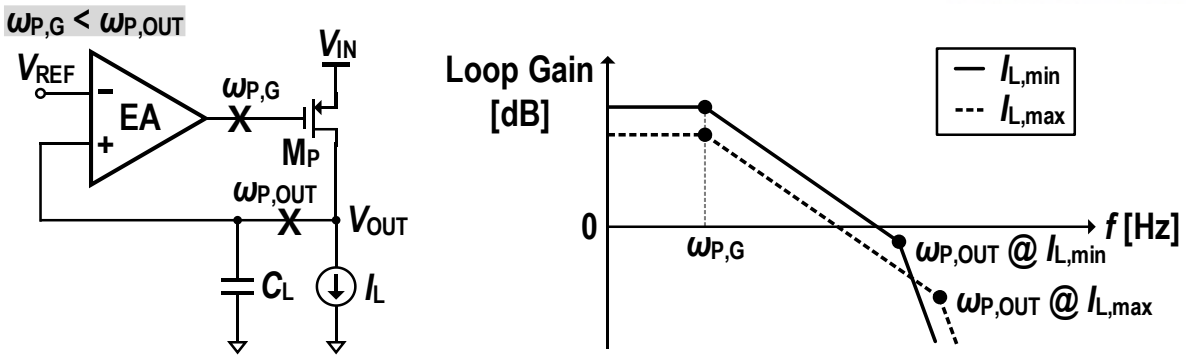


Figure 13. Stability issue at $I_{L,min}$ in GPD LDO.

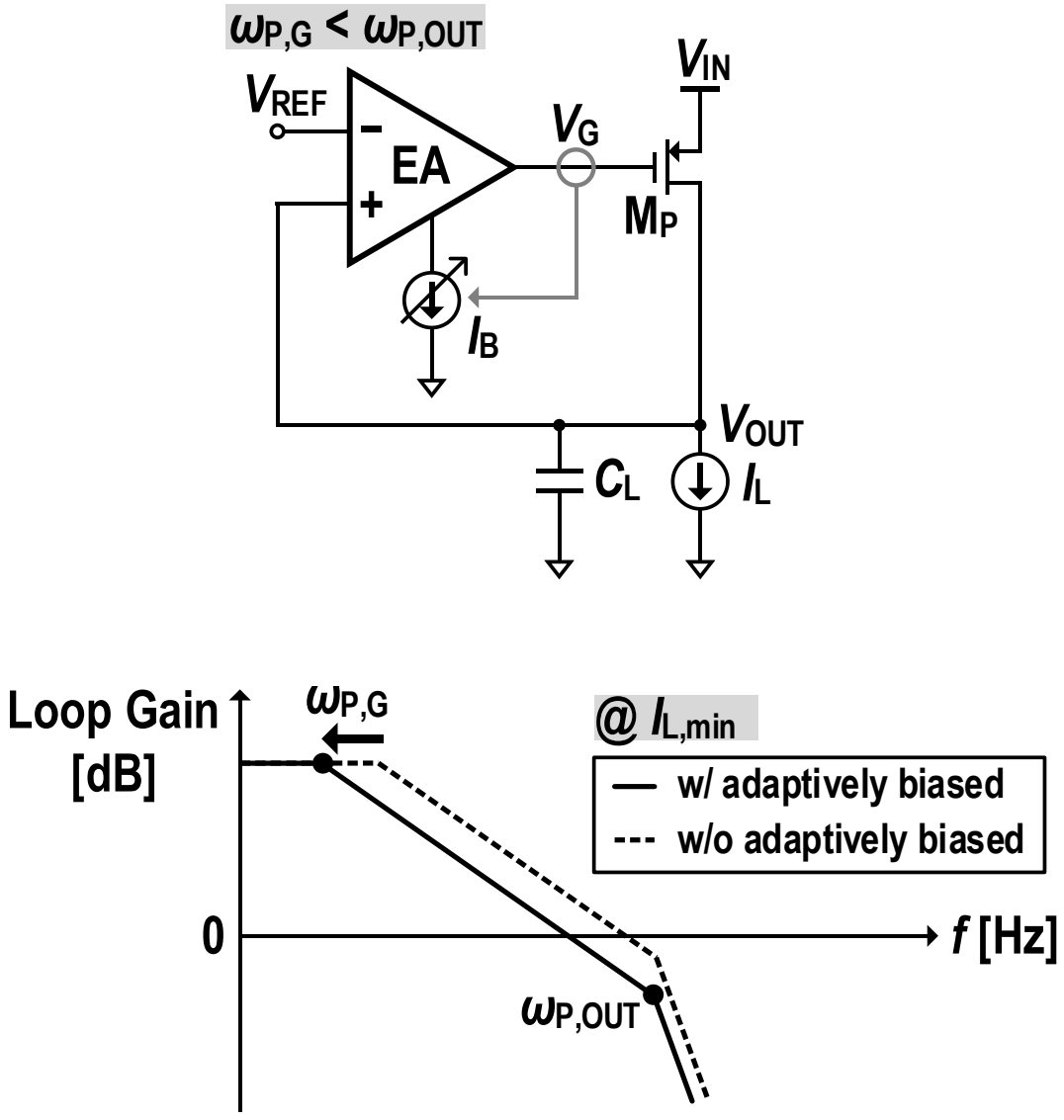


Figure 14. GPD LDO with adaptively biased EA.

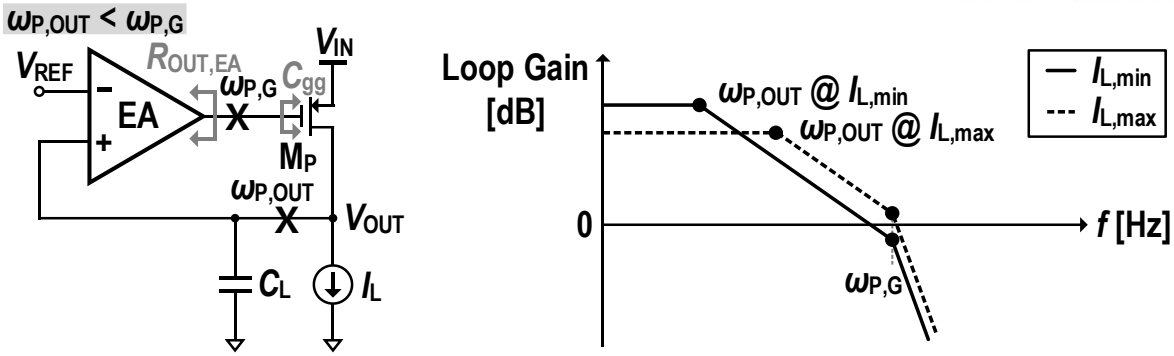


Figure 15. Stability issue at $I_{L,max}$ in OPD LDO.

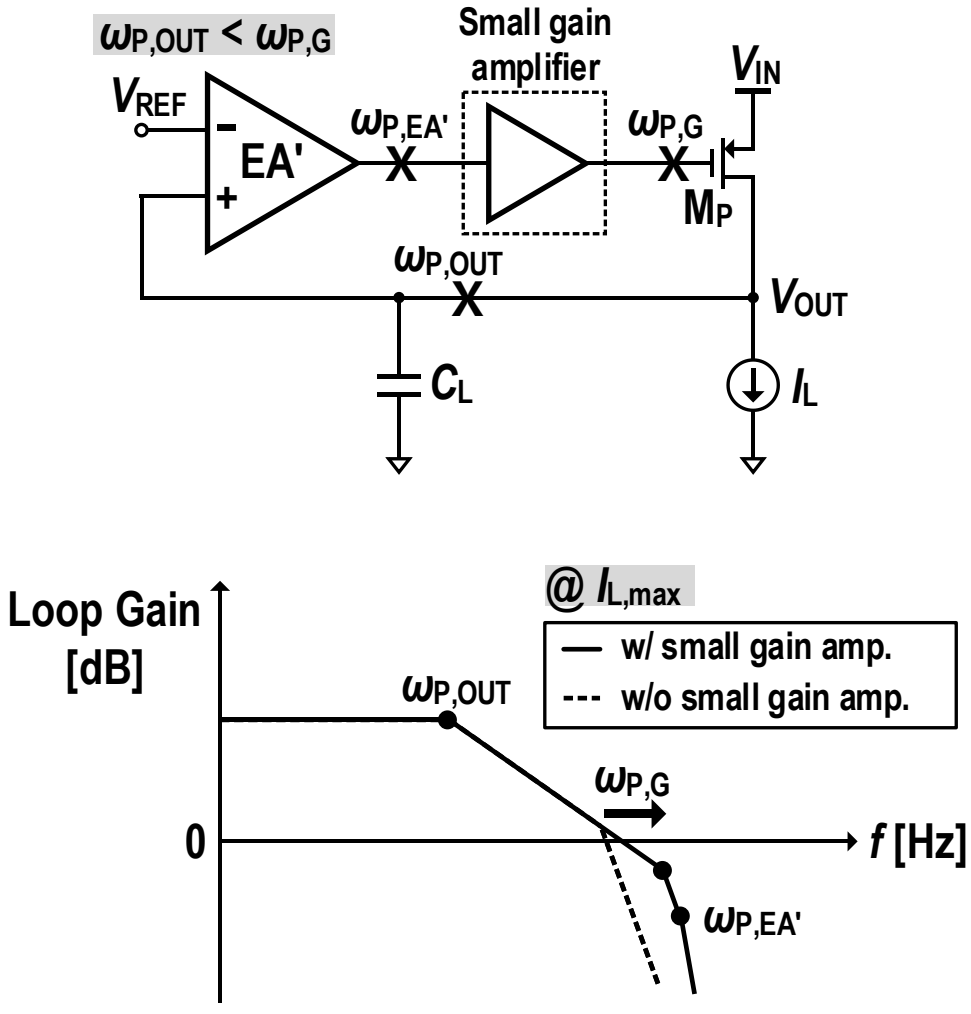


Figure 16. OPD LDO with small gain amplifier.

III. DESIGN AND SIMULATIONS OF AN ANALOG LDO

3.1 DESIGN OF AN ANALOG LDO

Analog LDOs are added in a chip for the loads that need noise-less supply such as VCOs and ADCs. In these applications, high PSRR and tight line and load regulation performance are necessary. The target specification as an analog LDO that has 50dB $A_{OL,DC}$ and 10kHz $BW_{OL,-3dB}$, 10μA I_Q, and 10pF C_L. The PSRR condition comes from DC/DC converter that supply the voltage to the LDO with 100mV_{P-P} switching ripple and 50kHz switching frequency. A load block is VCO that consumes 60mW power and needs 30mA total current in worst case of power. To make the power of the LDO as less than 10% of the load power, V_{DO} was chosen as 200mV.

Then, we can decide the size of M_P considering the W/L ratio should be large as it can drive target $I_{L,max}$ operating in saturation region. The W/L of M_P was designed as 3.8mm/30nm. In decision of the EA structure, we selected 1-stage NMOS-input PMOS mirror differential to single-ended EA for simplicity as shown in Figure 17. For increasing $R_{OUT,EA}$, we increased the length of transistors. For increasing $g_{m,EA}$ and widening output dynamic range, we increased the width of transistors.

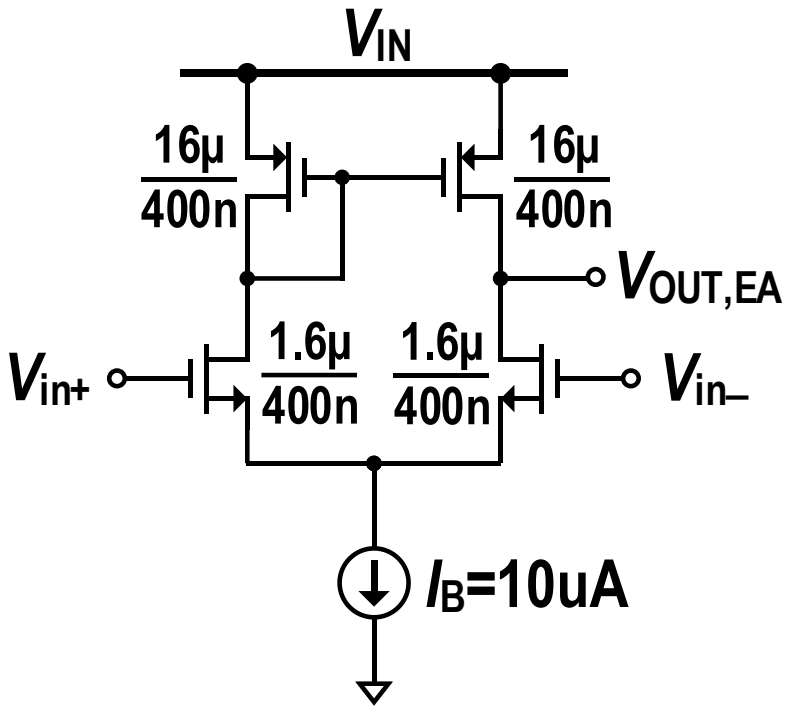


Figure 17. 1-stage NMOS-input PMOS-mirror EA

Designed EA has 40dB DC gain and 12MHz BW. If M_P is attached to this EA, the gain will increase and BW will be reduced. In Figure 18, a test bench is shown. By changing bias current of the load

controller (V_B), we can measure the transient response of the LDO. The structure of the load controller is shown in Figure 19. In this structure, for the load controller performing desired T_{edge}, we should pay attention to the parasitic capacitance (C_P) and resistance at the mirror pole since it can limit T_{edge} for RC delay at this node having much slower value than the one we expected. We designed the load controller can have 100ns T_{edge}.

3.2 SIMULATIONS OF AN ANALOG LDO

The transient response is shown in Figure 20. By using an iprobe, we investigated the open loop gain and phase of total system as shown in Figure 21. As we expected, the gain increased and BW_{-3dB} was reduced by attaching M_P. By injecting AC signals to supply, we found the PSR along frequency as shown in Figure 22. When a DC/DC converter has 100mV_{P-P} switching ripples and 50kHz switching frequency, this LDO can reduce the ripples as less than 1mV_{P-P} at the V_{OUT}.

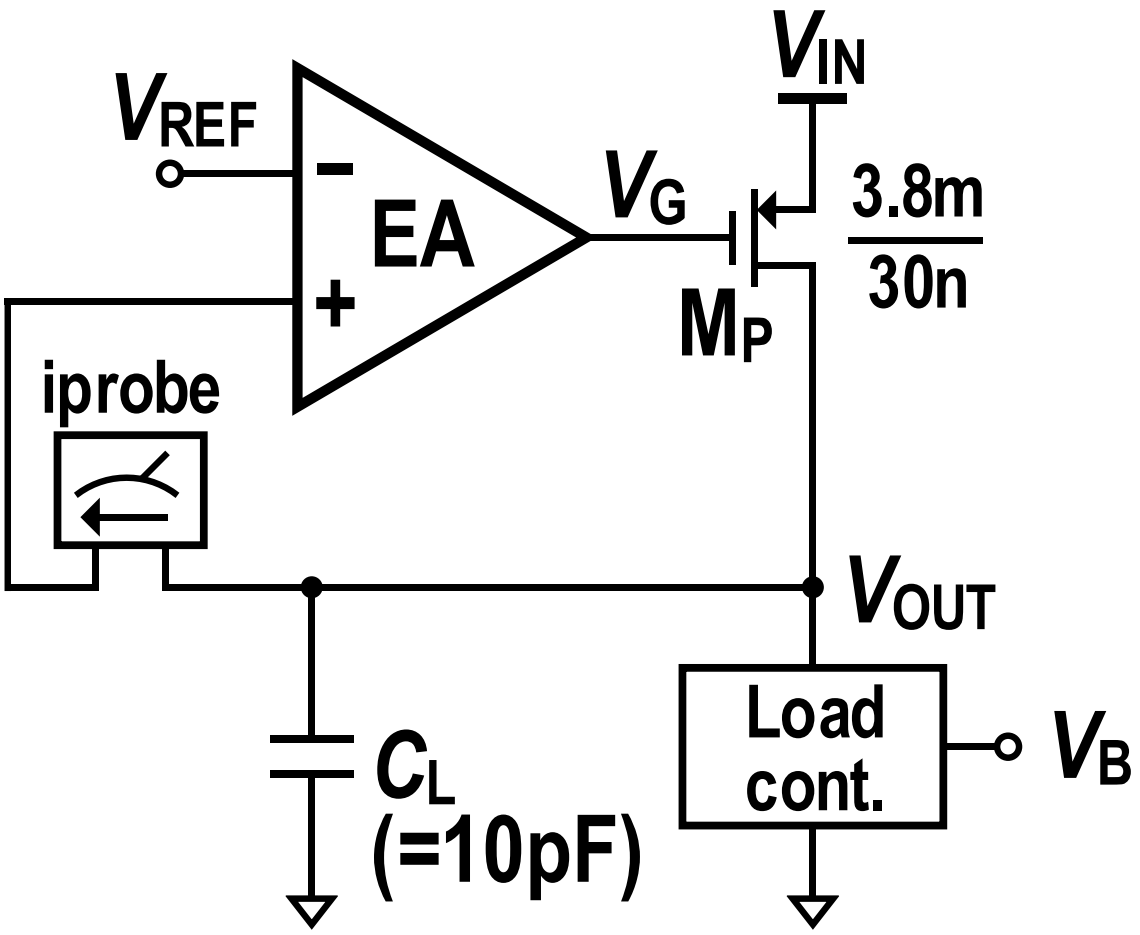


Figure 18. Test bench for designed analog LDO

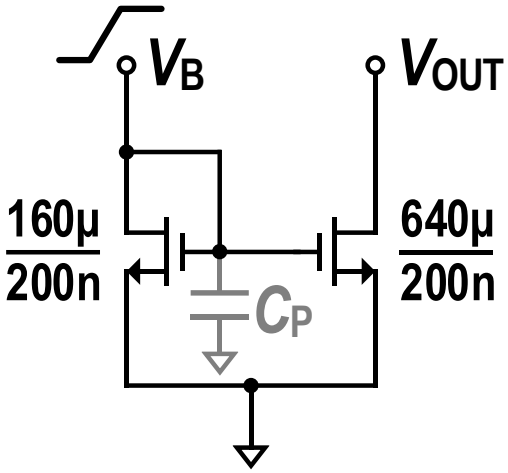
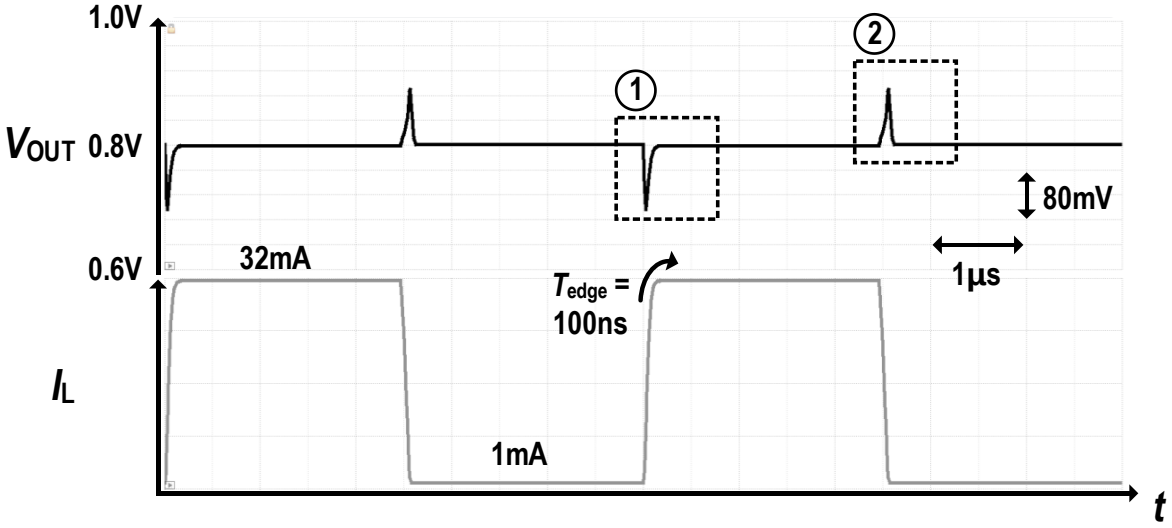


Figure 19. Load controller for designed analog LDO



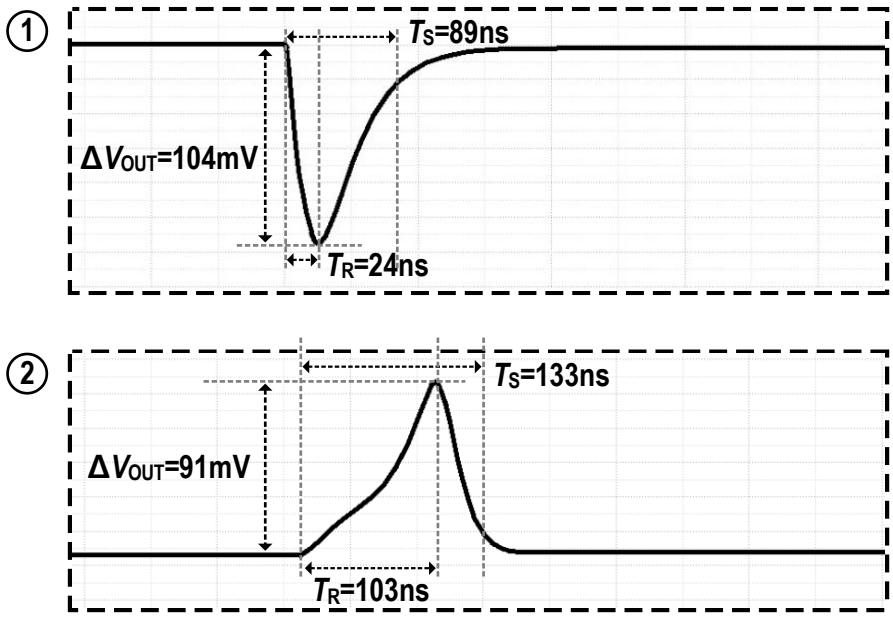


Figure 20. Load transient response of designed analog LDO

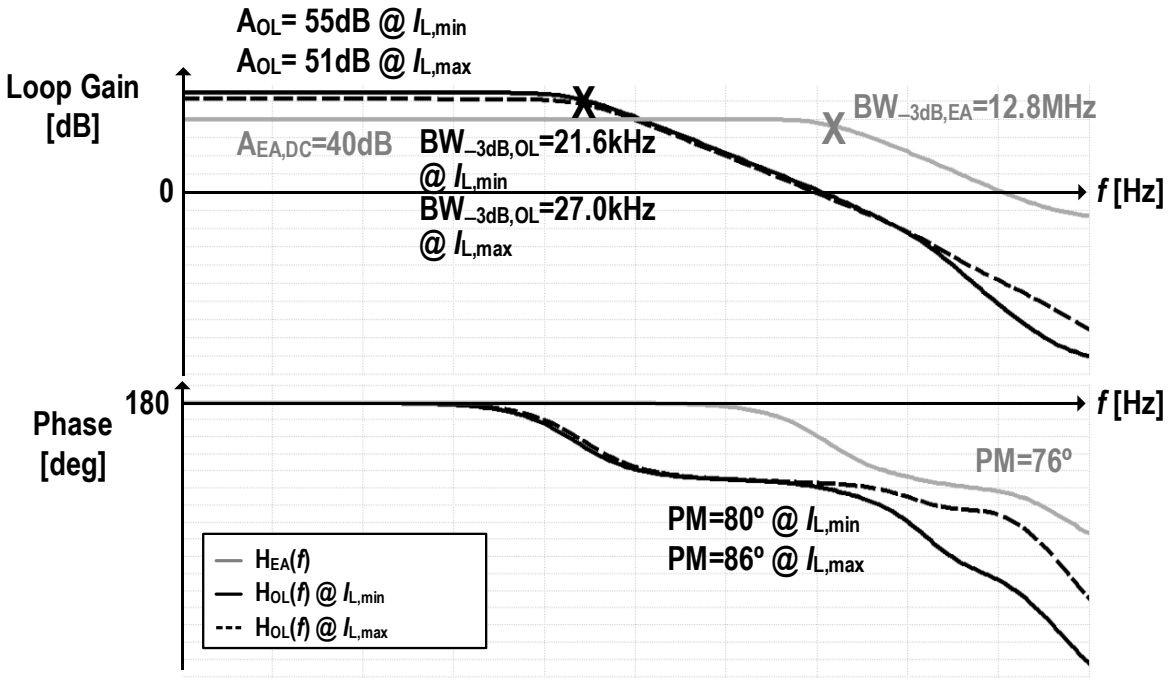


Figure 21. Transfer functions of designed analog LDO

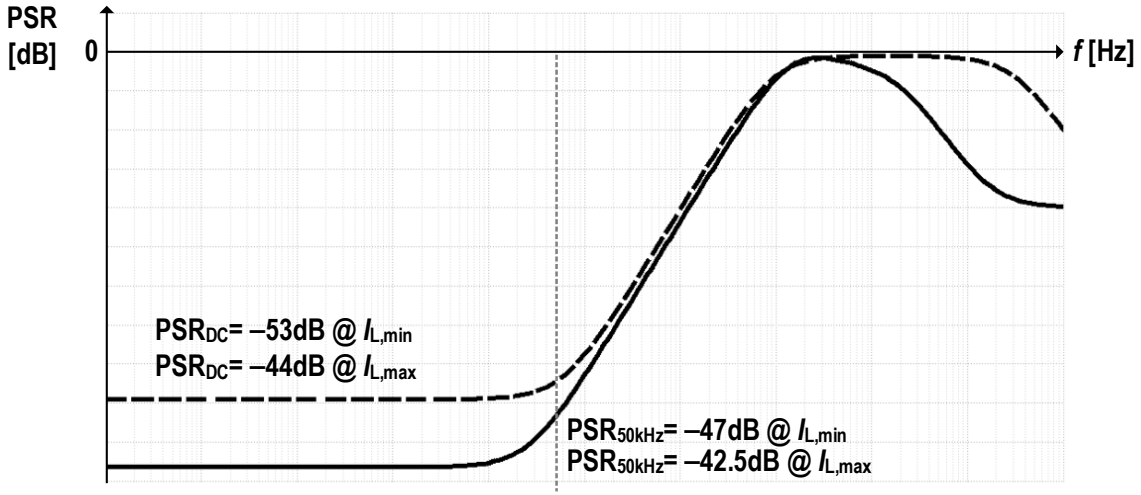


Figure 22. PSRR characteristics of designed analog LDO

If we need more gain in the low V_{IN} condition, as shown in Figure 23, a two-stage amplifier with a local positive feedback loop topology that makes R_{OUT} of PMOS part of 1st stage ideally infinite using negative g_m can be used [11]. It can increases slew rate and gain. However, if the W/L ratio of PMOSs in the positive feedback loop are larger than diode connected PMOSs in 1st stage, latching can occur. That means the output cannot change appropriately by the input since the g_m of local positive feedback transistors gets larger than the g_m of input transistors.

This two-stage topology brings another low frequency pole at the 1st stage, so we should remove it for keeping the LDO stable. We can add zero path between supply to the gate of M_P as shown in Figure 24 [12]. In this location, the transfer function of LDO can add zero to remove the pole of 1st stage output node using pole-zero cancellation (PZC) technique. It also makes high PSRR for C_Z helping V_G copy V_{IN} as mentioned in Section 2.2.1.

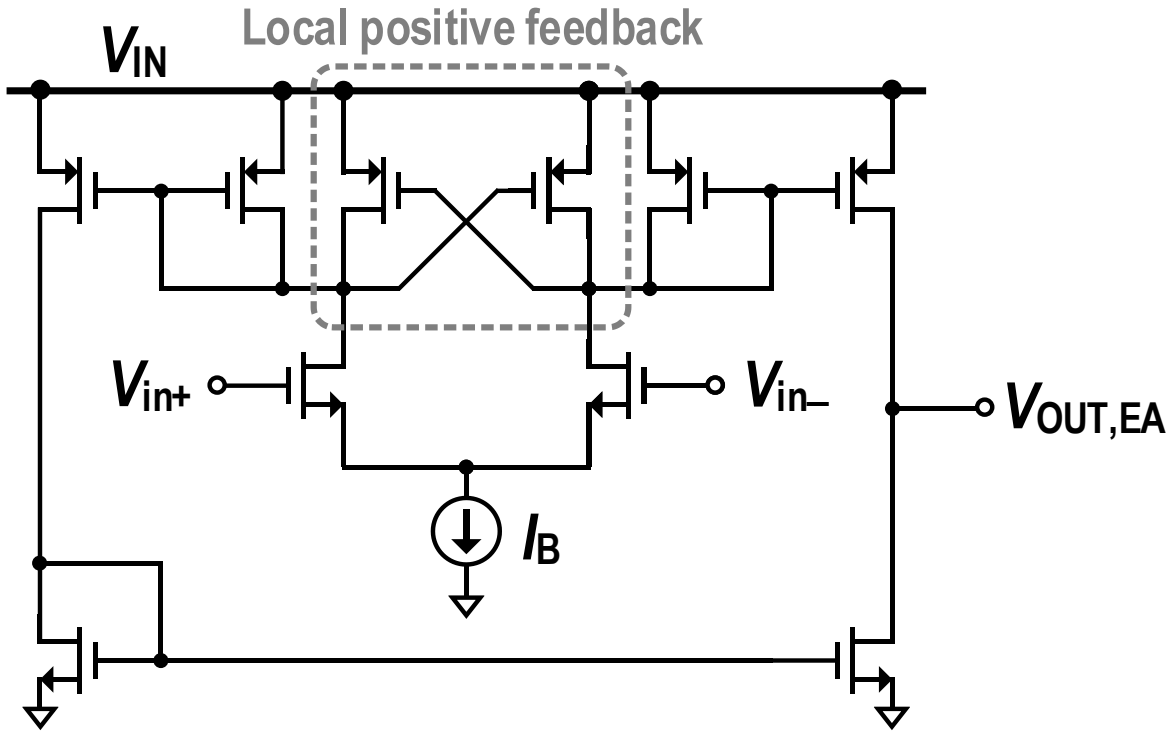


Figure 23. Two-stage amplifier with a local positive feedback loop

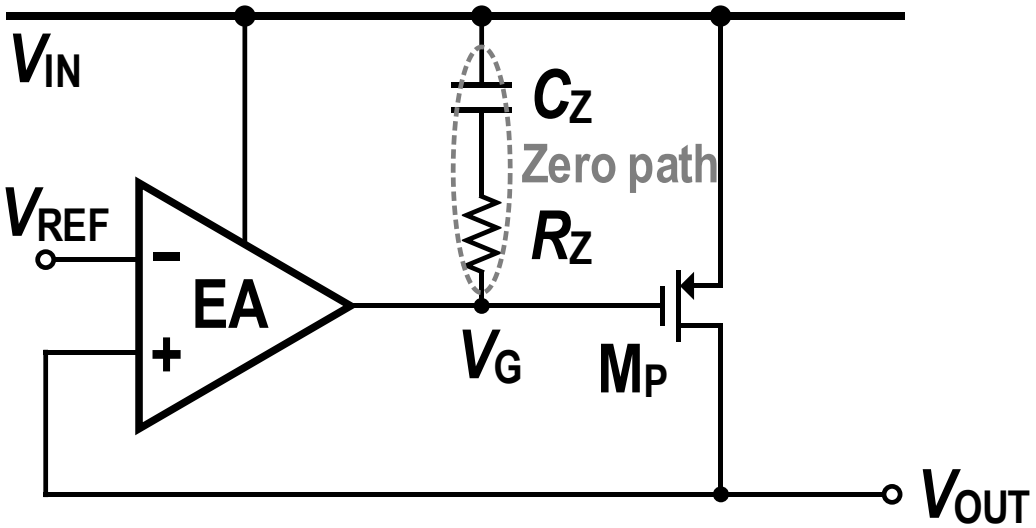


Figure 24. Added zero path for PZC and high PSRR.

We can consider about fast T_R analog LDO for applications such as a power-gating VCO in a fully-integrated chip. These applications need to rapidly change to frequent start-up. For improving the transient response of analog LDOs, a flipped-voltage-follower (FVF) can be used [3]. This technique contains problem in heavy load condition that is FVF pole can be seen as an added low frequency pole making the system unstable. Furthermore, increasing slew rate of FVF for fast response to large load change consumes huge amount of power. Thus, we can use that technique in only narrow I_L range situation.

IV. FUTURE WORK

4.1 MOTIVATION OF DIGITAL LDOS

In low supply applications, EAs can't have high gain. Thus, achieving high A_{OL} without EA is needed. One solution for this problem is digital LDO. As shown in Figure 25, basic digital LDOs consist of a comparator (COMP), a switch controller (SWC), and M_{PS}s that fully turn on and off. Since the M_{PS}s can provide large current operating in triode region, digital LDOs also get popular in memory loads that produce large I_L. We also take advantages such as low V_{DO}, comfortable integration with digital circuits, and process scalability. However, digital LDOs have disadvantages and limitations compared to analog LDOs. The comparison between analog and digital LDOs is written in Table 5.

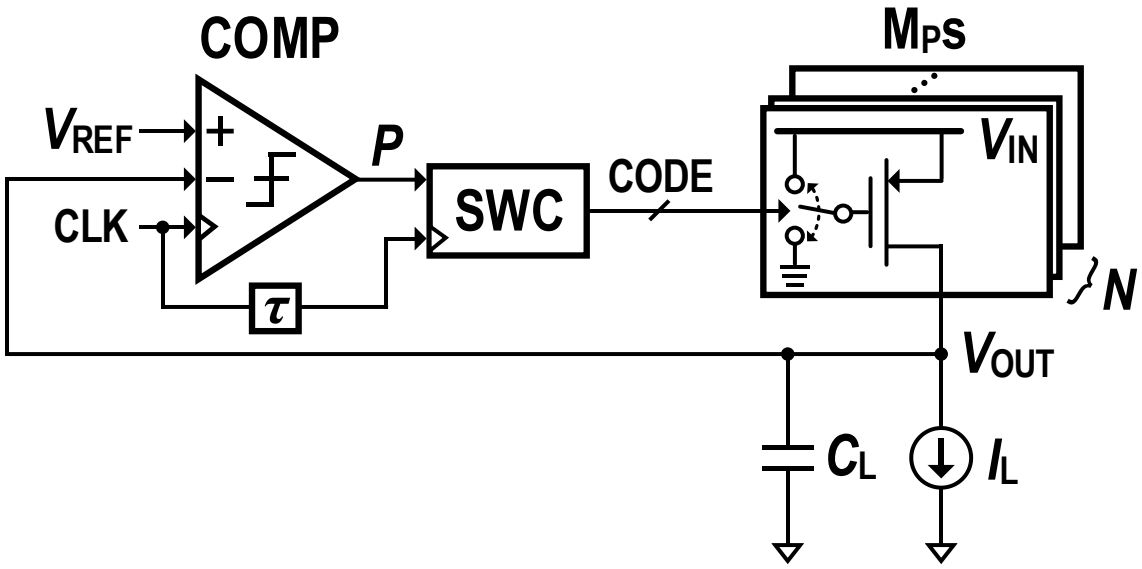


Figure 25. Basic digital LDO

In the PSRR of digital LDOs, if the v_R changes with the frequency slower than sampling frequency (F_S)/2, it can be compensated. The ripple amplitude of V_{OUT} can be reduced only as the current resolution of least significant bit (LSB) M_P of the LDO. Plus, the delay from sensing the ripple to update the control code of M_{PS}s worsens the PSRR of digital LDOs. Thus, PSRR of digital LDOs is typically poor than that of analog LDOs. Limited resolution of digital LDOs also affects the line and load regulation. The regulation performance stays coarse in digital LDOs.

Fast T_R can be achieved by continuous detection and high slew rate in OPD analog LDOs with large power. In GPD analog LDOs, slew rate is limited by the stability. In the digital LDOs, for reducing T_S, F_S can increase but it needs lots of I_Q. In [13], the LDO can response transition rapidly, but the steady-state power is reduced since F_S slows down automatically as the difference between V_{REF} and V_{OUT} gets

smaller. However, the sum of time taken to detect and propagation delay to updating the code of M_Ps cannot be reduced well. The T_R in worst case is $1/F_s$ + calculation delay as shown in Figure 26.

In the stability of digital LDO, since the SWC is commonly an accumulator that is a discrete-time integrator, it contains a pole at z=1 in z-domain, digital LDOs naturally classified as GPD LDO [14]. However, by the value of F_S, this system can be unstable causing limit cycle oscillation. The digital LDO in [13] mentioned earlier can also solve the stability problem by making the F_S slows down when the value enters the settling range.

In power and area, OPD LDOs have trade-off between power and area for securing PM, GPD LDOs don't need to increase I_G but should provide static current to EA and also don't need large C_L but the M_P size should be larger than digital LDO since M_P needs to operate in saturation region. In addition, V_{DO} of digital LDO can be small as about 50mV operating in triode region.

Table 5. Comparison of analog and digital LDO

	OPD analog LDO	**GPD analog LDO**	**Digital LDO**
PSRR	High PSRR @high freq.	High PSRR @low freq.	Low PSRR @all freq.
Line & load regulation	Medium	Fine	Coarse
T_R	Fast	Slow	Slow
T_S	Fast	Slow	Fast
Stability issue	@ $I_{L,max}$	@ $I_{L,min}$	@ $I_{L,min}$ & high F_S
Power	Large	Medium	Small
Area	Large	Medium	Small
Low supply operation	Poor	Poor	Good

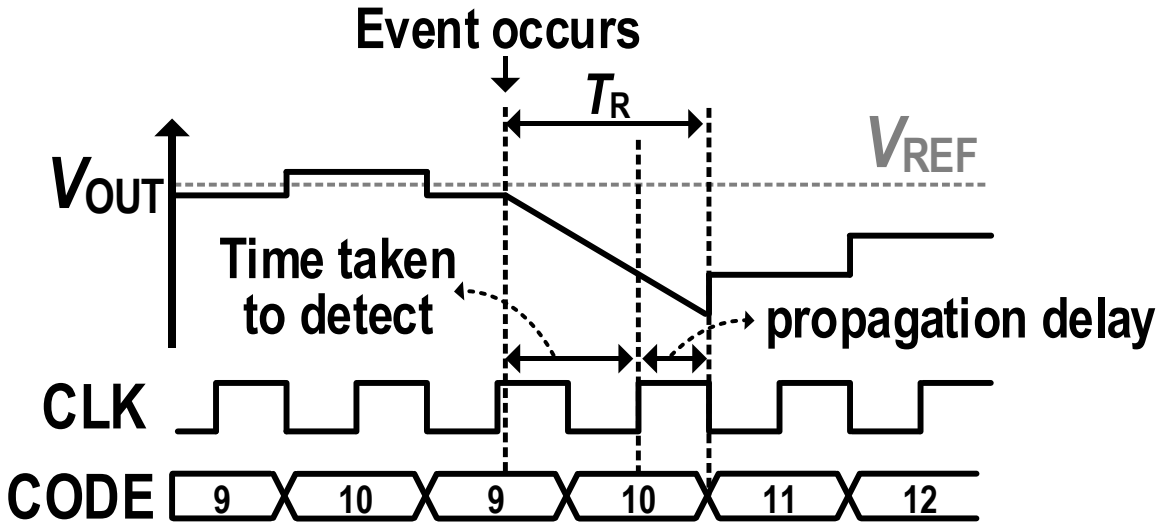


Figure 26. The timing diagram from detection to updating the code of M_Ps.

4.2 DIGITAL LDOS FOR FAST TRANSIENT AND HIGH ACCURACY

Digital LDOs are added in a chip for the loads that are frequently changing by input data sequences and lots of functions share one common V_{IN} from DC/DC converter output in a chip such as DRAM and CPU systems. For digital loads, if V_{OUT} droop is larger than the logic threshold value, it can evoke critical errors in operation. Thus, in the frequently changing I_L with changing the logic levels, keeping V_{OUT} droop is one of most significant goals in digital loads. Plus, little decrease in V_{OUT} that is supply of the logic gates makes the speed of calculation of digital logics go slow down.

In these application, digital LDO should have fast transient response and wide I_L range. There is a trade-off between transient response and power. To break this trade-off, adaptive F_S techniques are introduced [13–14]. If we want to compensate the current in a few cycles regardless of the speed of F_S, ADC is needed since it can expect the amount of the change of I_L. However, depending on the number of the level of the ADC, it has trade-off between resolution and power & area.

Moreover, even the ADC gives exact information about ΔV_{OUT}, this ΔV_{OUT} can be the result of different ΔI_Ls. In other words, the result cannot exactly detect the difference of I_{LDO} and I_L, that is how many transistors should be turned on. This is because the voltage difference has the relationship with ΔI_L as written in (11), where $I_{L,initial}$ is the I_L that is initially provided in steady-state before the transition. It is worth nothing that this equation assumes that there is only R_L and ignore C_L, but in real, two components can affect ΔV_{OUT}.

$$\Delta V_{OUT} \propto I_{L,initial} \cdot \Delta I_L \tag{11}$$

By (11), we can know that $I_{L,initial}$ affects the ΔV_{OUT} as well as ΔI_L. For example, as shown in Figure 27, ΔV_{OUT}=10mV can be the result of 3→10mA or 1→5mA.

One technique to reduce T_S without mixed solutions is binary search algorithm [15]. However, it can evoke overcompensation and glitches. This is because even in the small ΔI_L, binary search should starts changing as $I_{L,max}/2$.

Another unsolved problem in these fast T_S digital LDOs is that T_R cannot be reduced as shown in Figure 26. Event-driven digital LDO can reduce T_R, but it needs consistent power.

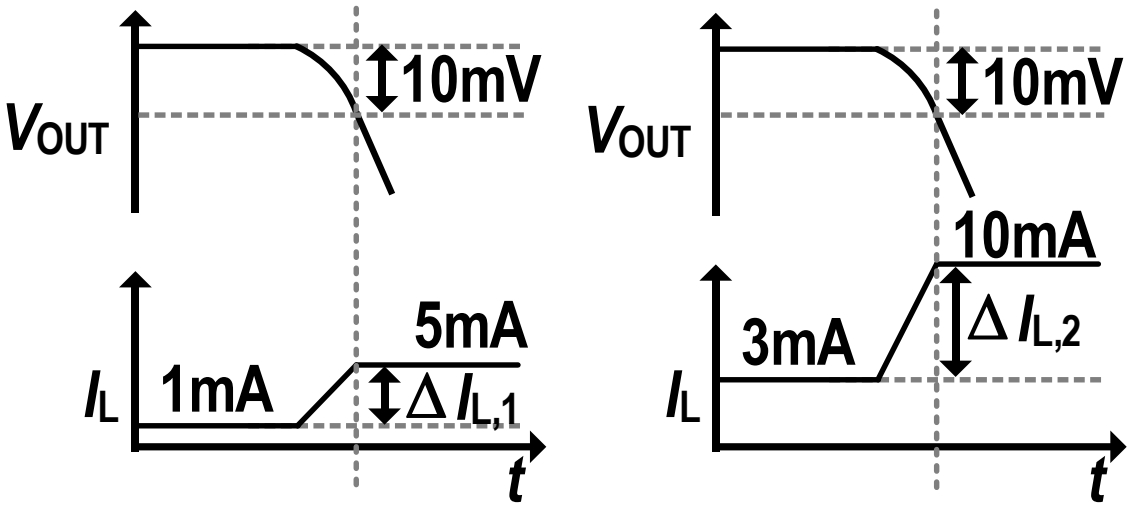


Figure 27. Same voltage difference by two different I_L step conditions

For DVFS applications, the accuracy of digital LDOs can be a crucial factor. For improving the accuracy where the fine-grain DVFS is needed for SoC demanding <10mV voltage resolution [6], the techniques such as switched-capacitor resistance with high frequency [6], 1-bit DSM [16], and multi-level V_G generator [17] can be used.

4.3 HYBRID LDOS FOR FAST TRANSIENT AND HIGH PSRR

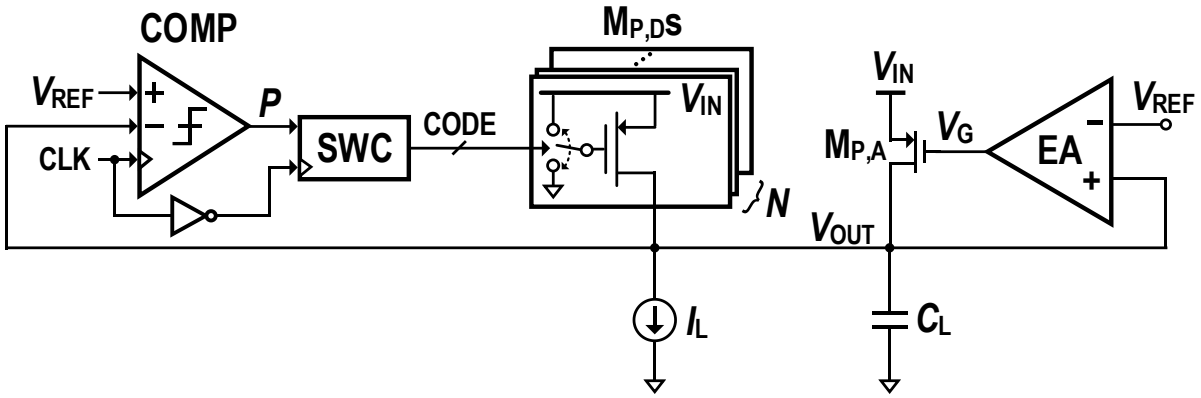


Figure 28. Analog-digital hybrid LDO

In some SoC applications, one wants to use same LDO for both analog and digital loads for design convenience and ordered floorplan. For these applications, a LDO that can drive both analog and digital loads is crucial. For that, a LDO should be versatile that can rapidly respond to the load transient, achieve high PSRR in a fully-integrated chip. Recent analog-digital hybrid LDOs usually focuses on the fast transient and moderate PSRR performance [18–19], but achieving high PSRR remains a critical problem for analog loads. Plus, since OPD and GPD analog LDOs have different characteristics, there are problems with OPD or GPD based hybrid LDO topology respectively.

In [18], an OPD analog + digital LDO is introduced. They insist that if load needs fast settling to large ΔI_L, added digital LDO can compensate these performances. However, there are problems such as they can degrade the size merit of digital LDO by large C_L and the accuracy cannot be much improved by stability issue when increasing A_{EA}.

In [19], a GPD analog + digital LDO can have high accuracy with digital integrator regulating steady-state error. Since the error regulation needs slow F_S, it consumes small power. Both GPD and digital LDO require high $\omega_{P,OUT}$, area can be kept small. However, it cannot response to the load change rapidly due to stability issue when increasing I_G in GPD analog LDO and limitation of delay in digital LDO as mentioned earlier in Figure 26.

In the fully-integrated circuit, the GPD analog + digital LDO topology can be more attractive option. However, this topology needs the way to respond rapidly to the load transient without sacrificing power and degrading PM. Furthermore, the problem of degradation in PSRR still exists.

V. CONCLUSIONS

In SoC applications, LDOs are needed for reducing switching ripples from high-efficiency regulators and spurs from other loads sharing the same regulators, and providing different supply voltages to different loads. When designing LDOs, choosing proper type in pass transistor, EA, and dominant pole along with applications is crucial. For designing LDOs, building reasonable priority is important starting from obtaining target specifications.

In analog LDOs, we deal with advanced techniques such as local positive feedback loop and zero path that improves stability and PSRR performance. OPD LDO has large C_L and GPD LDO has slow T_R and T_S. For fully-integration, GPD LDO is preferred but slow transient responses should be improved.

In digital LDOs, the techniques that make T_R and T_S fast are introduced. Adaptive F_S for improving T_R and T_S needs to clock generating high F_S. ADC-based voltage comparators for improving T_S have ambiguous answer problem that one ΔV_{OUT} information contains lots of solutions about ΔI_Ls. Plus, the techniques that make fine resolution of I_{LDO} are introduced.

In analog-digital hybrid LDOs, for both analog and digital loads in a fully-integrated chip, GPD+digital LDO combination is preferred than OPD+digital combination with moderate PSRR performance and high accuracy. Also, we can improve T_S with a digital LDO. However, degradation of PSRR from $M_{P,D}$s of a digital LDO remains a problem. Furthermore, slow T_R from both stability issue in GPD LDO and clock-dependent tendency in digital LDO should be improved.

REFERENCES

[1] Maxim Integrated, "Tutorial: Regulator Topologies for Battery-Powered Systems," Jan. 2001.

[2] V. Gupta, G. A. Rincón-Mora, and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," *Proceedings - IEEE International SOC Conference*, no. 1, pp. 311–315, 2004.

[3] Y. Lim, J. Lee, S. Park, Y. Jo, and J. Choi, "An External Capacitorless Low-Dropout Regulator with High PSR at All Frequencies from 10 kHz to 1 GHz Using an Adaptive Supply-Ripple Cancellation Technique," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2675–2685, 2018.

[4] Y. Lu, W. H. Ki, and C. P. Yue, "A 0.65ns-response-time 3.01ps FOM fully-integrated low-dropout regulator with full-spectrum power-supply-rejection for wideband communication systems," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, vol. 57, pp. 306–307, 2014.

[5] B. M. King, "Advantages of using PMOS-type low-dropout linear regulators in battery applications," *Texas Instrument, Analog Application Journal*, pp. 16–21, Aug. 2000.

[6] L. G. Salem and P. P. Mercier, "A sub-1.55mV-accuracy 36.9ps-FOM digital-low-dropout regulator employing switched-capacitor resistance," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, vol. 61, pp. 312–314, 2018.

[7] S. Bu, K. N. Leung, Y. Lu, J. Guo, and Y. Zheng, "A Fully Integrated Low-Dropout Regulator with Differentiator-Based Active Zero Compensation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 10, pp. 3578–3591, 2018.

[8] B. S. Lee, "Application Report: Understanding the Terms and Definitions of LDO Voltage Regulators," *Texas Instrument*, Oct. 1999.

[9] C. Zhan and W. H. Ki, "Output-capacitor-free adaptively biased low-dropout regulators," *2010 IEEE International Conference of Electron Devices and Solid-State Circuits, EDSSC 2010*, vol. 57, no. 5, pp. 1017–1028, 2010.

[10] M. Ho, K. N. Leung, and K. L. Mak, "A low-power fast-transient 90-nm low-dropout regulator with multiple small-gain stages," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 11, pp. 2466–2475, 2010.

[11] J. Roh, S. Byun, Y. Choi, H. Roh, Y. G. Kim, and J. K. Kwon, "A 0.9-V 60-μW 1-bit fourth-order delta-sigma modulator with 83-dB dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 361–370, 2008.

[12] X. Liu *et al.*, "A Modular Hybrid LDO with Fast Load-Transient Response and Programmable PSRR in 14nm CMOS Featuring Dynamic Clamp Tuning and Time-Constant Compensation," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, vol. 62, pp. 234–236, 2019.

[13] J. Lee *et al.*, "A 0.5V-V_{IN}, 0.29ps-transient-FOM, and sub-2mV-accuracy adaptive-sampling digital LDO using single-VCO-based edge-racing time quantizer," *IEEE Symposium on VLSI Circuits*, pp. 130-131, Jun. 2019.

[14] S. Bin Nasir, S. Gangopadhyay, and A. Raychowdhury, "All-Digital Low-Dropout Regulator with Adaptive Control and Reduced Dynamic Stability for Digital Load Circuits," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8293–8302, 2016.

[15] L. G. Salem, J. Warchall, and P. P. Mercier, "A Successive Approximation Recursive Digital Low-Dropout Voltage Regulator with PD Compensation and Sub-LSB Duty Control," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 1, pp. 35–49, 2018.

[16] H. Song, W. Rhee, I. Shim, and Z. Wang, "Digital LDO with 1-bit ΔΣ modulation for low-voltage clock generation systems," *Electronics Letters*, vol. 52, no. 25, pp. 2034–2036, 2016.

[17] Y. Lim, J. Lee, Y. Lee, S. Yoo, and J. Choi, "A 320μV-Output Ripple and 90ns-Settling Time at 0.5V Supply Digital-Analog-Hybrid LDO Using Multi-Level Gate-Voltage Generator and Fast-Decision PD Detector," *IEEE European Solid State Circuits Conference*, vol. 44, pp. 94–97, 2018.

[18] S. Bin Nasir, S. Sen, and A. Raychowdhury, "Switched-Mode-Control Based Hybrid LDO for Fine-Grain Power Management of Digital Load Circuits," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 2, pp. 569–581, 2018.

[19] M. Huang and Y. Lu, "An Analog-Proportional Digital-Integral Multi-Loop Digital LDO with Fast Response, Improved PSR and Zero Minimum Load Current," *IEEE Custom Integrated Circuits Conference*, 2019.

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